Energy 77 (2014) 591–596

Contents lists available at ScienceDirect

Energy

journal homepage: www.elsevier.com/locate/energy

Synergistic effect between ordered $Bi_2Te_{2.7}Se_{0.3}$ pillar array and layered Ag electrode for remarkably enhancing thermoelectric device performance

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ARTICLE INFO

Article history:
Received 28 April 2014
Received in revised form
21 August 2014
Accepted 14 September 2014
Available online 6 October 2014

Keywords:
Pillar array
Layered electrode
Synergistic effect
Micro-device
Thermoelectric performance

ABSTRACT

In this study, it was found that a remarkably enhanced performance could be achieved in pillar array device with layered electrode through coordinate regulation between thermoelectric pillar array and layered electrode structures. The highly ordered vertical *n*-$Bi_2Te_{2.7}Se_{0.3}$ pillar array and layered structure Ag films were fabricated by a magnetron sputtering method. The measurement result showed that the $Bi_2Te_{2.7}Se_{0.3}$ pillar array and the layered Ag film were beneficial for improvement of in-plane properties, being a promising choice for planar micro-devices. These films have been integrated into low-dimension planar devices using mask-assisted deposition technology. The performance of the pillar array device with layered Ag film electrode has been tested, which was very superior to that of the pillar array device with ordinary structure electrode. For the typical 38 legs device with layered structure electrode, the output voltage and maximum power were up to 12.4 mV and 16.02 μW, respectively, for a temperature difference of 65 K. The device could produce a 11.1 K maximum temperature difference at current of 50 mA. Our results demonstrated a route to tailor unique thermoelectric pillar array and layered electrode nanostructure inside micro-devices so as to effectively improve device performance.

1. Introduction

Solid-state TE (thermoelectric) generator and cooler composed of *n* or/and *p* semiconductor elements can be used for conversion of heat to electricity, and vice versa. Their great potential in providing cleaner form of energy and reducing environmental contamination has been widely recognized [1–5]. Many different approaches have been proposed and attempted to improve the performance of such devices [6,7]. Solid-state power generation and cooling devices have recently shown promising prospects through use of low-dimensional nanostructured TE materials, among which Sb–Bi–Te materials are most frequently studied; for examples, Francioso et al. [8] reported that a 100-pair thermocouple TE generator could produce a maximum open-circuit voltage (V_{op}) of 430 mV and estimated output power (P_{max}) of 32 nW at temperature difference (ΔT) of 40 K. Kim et al. [9] have fabricated a 242-pair thermocouple generator which could exhibit V_{op} of 294 mV and P_{max} of 5.9 μW at $\Delta T = 22.3$ K. Snyder et al. [10] have prepared that 126-pair couples for a device operating in power-generation mode to produce $P_{max} = 1$ μW on illumination by a lamp. Huang et al. [11] showed that a 200-pair cooler would produce a 1.2 K maximum temperature difference (ΔT_{max}) at current of 200 mA. Silva et al. [12] fabricated a micro TE cooler with 60 pairs of *n*-*p* elements which could produce a ΔT_{max} of 1.3 K at an operating current of 23 mA. These reported devices have some other advantages, for example, excellent V_{op} and good design concept, but with the drawback of low *ZT* values of TE materials and parasitic series resistances. However, the pillar array structure can help to improve the TE figure-of-merit, and the layered structuring process possibly induces a favorable change in the Fermi surface topology of electrode to improve the problems.

Here, $Bi_2Te_{2.7}Se_{0.3}$ pillar array is expected to be high *ZT* value at room temperature because of its unique build-up structure, and layered Ag film is introduced into a planar device as electrode (reducing Joule heating and improving thermal transport) using magnetron sputtering, which can greatly improve electrical and thermal transport and dramatically enhance performance of a planar micro-device with $Bi_2Te_{2.7}Se_{0.3}$ pillar array legs. To the best of our knowledge, ordered $Bi_2Te_{2.7}Se_{0.3}$ pillar array micro-device with layered Ag electrode has been not reported to date. The

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http://dx.doi.org/10.1016/j.energy.2014.09.041
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purpose of this paper is to provide a proof of principle demonstrating that ordered TE pillar array and layered structure electrode can be integrated into low-dimensional TE planar devices using a simple magnetron sputtering and mask-assisted deposition technology. Our goal here is to improve the power generation and cooling performance of such devices. Moreover, we also aim to obtain further insight into the relation between device microstructure and device performance. It is also the main emphasis on synergistic effect between ordered $Bi_2Te_{2.7}Se_{0.3}$ pillar array and layered Ag electrode for remarkably enhancing thermoelectric device performance. Such synergistic effect provides valuable information for the construction of various TE devices and provides guidance for thermal management applications requiring simultaneous control over electrical and thermal conductivities. This technology can be extended to the case of dynamic hot spots by integrating the multiple TE devices that can be switched on and off depending on the chip is in critical need of cooling/heating or fully utilizing the thermal energy of hot spots for power generation.

2. Experimental section

In this work, *n*-$Bi_2Te_{2.7}Se_{0.3}$ pillar array was grown on SiO_2 substrate with thickness of 0.25 mm at 350 °C deposition temperature in a magnetron sputtering system. Before deposition, the SiO_2 substrates were cleaned thoroughly by diluted nitric acid and acetone, and dried under the nitrogen airflow. Commercial 60-mm-diameter hot-pressed $Bi_2Te_{2.7}Se_{0.3}$ (99.99% purity), Se (99.99% purity) and Te (99.99% purity) targets (Purchased from General Research Institute for Nonferrous Metals, China) were used for co-sputtering to compensate for evaporated Se and Te at high temperature. The $Bi_2Te_{2.7}Se_{0.3}$ target was connected to a DC (direct-current) power supply with power of 30 W; while the Te target was connected to a radio-frequency power supply with power of 25 W; the Se target was connected to a DC power supply with corresponding power of 14 W. An Ag target (99.99% purity) was sputtered using target power of 35 W to deposit the layered and the ordinary Ag electrodes at 350 °C and 250 °C deposition temperature, respectively. The base pressure was lower than 2×10^{-4} Pa, and the working pressure of argon was fixed at 1 Pa.

Stainless steel masks with designed patterns were used to fabricate devices connected electrically in parallel, including masks for the TE film (mask$_f$) and electrode (mask$_e$), respectively. The process sequence and schematics of the fabricated TE device were presented in Ref. [13]. The size of the parallel device is 22 mm × 10 mm, with each TE element being 2.5 mm × 0.2 mm in area. $Bi_2Te_{2.7}Se_{0.3}$ pillar array was first deposited onto the SiO_2 substrate under mask$_f$, then Ag electrode was sputtered onto the substrate with the TE film using mask$_e$. All TE films were grown to thickness of 2 μm, and the electrode thickness was controlled to 500 nm by adjusting the deposition rate and sputtering time.

The crystal structures of the $Bi_2Te_{2.7}Se_{0.3}$ pillar array was examined by x-ray diffraction (XRD, Rigaku D/MAX 2200) using Cu K_α radiation (λ = 0.154056 nm). The films and legs morphology were observed by field-emission scanning electron microscopy (FE-SEM, Sirion 200). The compositions were detected by EDX (energy dispersive x-ray spectroscopy). Surface profilometry (Ambios XP-2, USA) was used to measure the film thickness. The electrical conductivity and Seebeck coefficient of the films were measured using a ZEM-3 (Ulvac Riko, Inc.) with a self-made test holder for film measurement in the in-plane direction. The in-plane thermal conductivity data were collected using a Laser PIT (Ulvac Riko, Inc.) at room temperature. The principle of the measurement method is described by Kato et al. [14] in detail. The carrier concentration and mobility were determined using a four-probe measurement based on the Hall effects (ECOPIA HMS-3000) at room temperature. We also measured the overall resistances of the TE micro-devices by a voltammetry method. The output voltages of the devices were measured by a DC digital voltage/current meter (Shanghai SB-2238) while applying a temperature difference between the hot and cold sides of the devices.

3. Results and discussion

$Bi_2Te_{2.7}Se_{0.3}$ pillar array was synthesized by a simple magnetron co-sputtering technique, achieving preferred growth at 350 °C deposition temperature and 1 Pa working pressure. The XRD pattern of the $Bi_2Te_{2.7}Se_{0.3}$ pillar array is shown in Fig. 1. All peaks could be indexed to rhombohedral phase $Bi_2Te_{2.7}Se_{0.3}$ material (JCPDS 50–0954). Compared with the standard card, the intensity of (0 1 5) peak of $Bi_2Te_{2.7}Se_{0.3}$ is dramatically strong, indicating highly preferential orientation of the film along the (0 1 5) direction. Besides, (0 0 15) texture is weak. The intense and sharp XRD peaks from the $Bi_2Te_{2.7}Se_{0.3}$ film are typical signatures of a high degree of crystallinity. They reveal a single-phase product with slightly broadened reflections, which is typical for crystals with low dimensions. $Bi_2Te_{2.7}Se_{0.3}$ resulting from this growth process is not necessarily epitaxially attached to the glass substrate. The atomic interactions between the $Bi_2Te_{2.7}Se_{0.3}$ atoms and the atoms of the amorphous SiO_2 substrate can locally obstruct the formation of a perfect crystalline order. In thin films growth, however, the growth kinetics can be influenced by temperature and working pressure. The deposited atoms have some energy for movement on the surface, leading to atoms to overcome surface diffusion barriers, which may be beneficial for migration of deposited atoms to preferred sites for textures growth; that is, crystallites nucleating with the thermodynamically preferred (0 1 5) orientation can grow, thus tending to realize highly preferential growth in the direction at the selected depositing conditions. It may be speculated that the strong (0 1 5)-oriented lattice may allow some preferential route for carrier transport, enhancing the carrier mobility and electrical conductivity in the pillar array. This plays a positive role on the power factors of the $Bi_2Te_{2.7}Se_{0.3}$ pillar array.

The $Bi_2Te_{2.7}Se_{0.3}Te_3$ pillar array is clearly shown by SEM images in Fig. 2. When viewed from the top (Fig. 2a), the pillar array appears to be relatively dense and uniform, and the surface topography of the film is composed of nano-grains. From the cross-sectional view of the film (Fig. 2b), we can observe that a large number of $Bi_2Te_{2.7}Se_{0.3}$ pillars have densely grown perpendicular to the substrate, along their preferential growth direction. The observation of ordered growth is also in agreement with the XRD

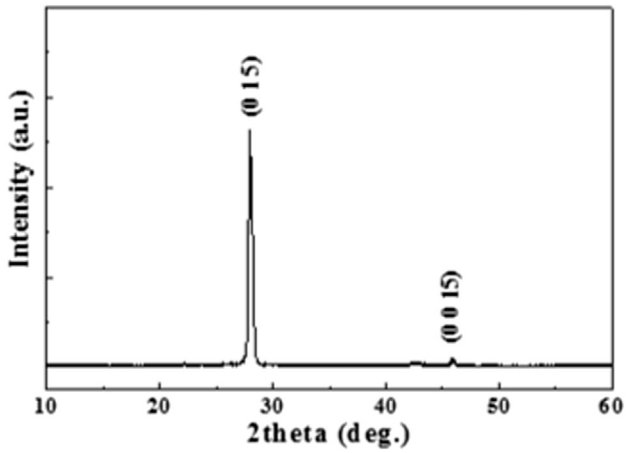

Fig. 1. XRD patterns of $Bi_2Te_{2.7}Se_{0.3}$ pillar array.

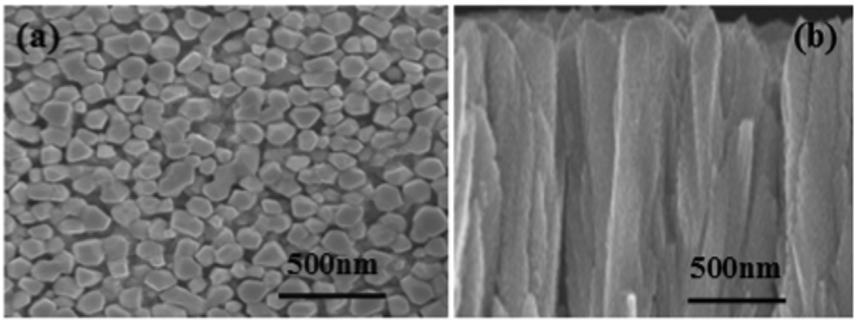

Fig. 2. (a) Surface view and (b) cross-sectional view of $Bi_2Te_{2.7}Se_{0.3}$ pillar array.

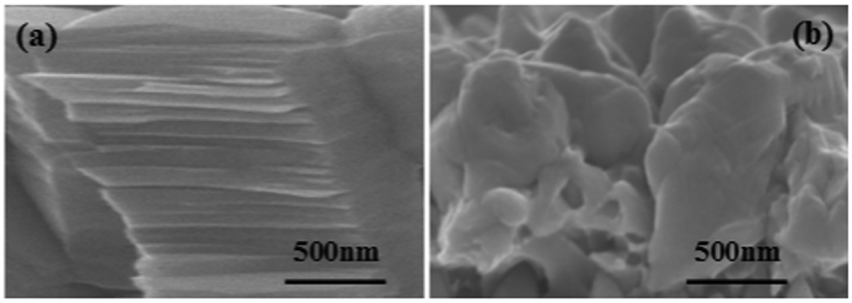

Fig. 3. SEM images of (a) layered and (b) ordinary Ag films with cross-sectional view.

analysis above. The sizes of pillars are uniform in the $Bi_2Te_{2.7}Se_{0.3}$ film. The diameters of pillars are estimated to be < 100 nm (Fig. 2b), implying numerous periodic interfaces in the film. At 350 °C deposition temperature and 1 Pa working pressure, the crystal growth in the radial direction is much faster than that of the planar direction. Simultaneously, the atoms on and near the surfaces of pillars will lose some neighbor atoms and electronic density. This will destroy the balance of these atoms, leading to interfaces and strained state. The interfaces and strained state are mainly responsible for the formation of the pillar array structure. As shown in Figs. 1 and 2, it exhibits that the (0 1 5)-preferential growth is the essential reason for the formation of the ordered $Bi_2Te_{2.7}Se_{0.3}$ pillar array. It seems reasonable to assume that the in-plane thermal conductivity of the $Bi_2Te_{2.7}Se_{0.3}$ pillar array is low, as expected on the basis of the novel structure. This is the fact that the high density of roughly periodic interfaces may produce thermal barriers with low thermal conductivity in the pillar array. The reduced thermal conductivity will also benefits from these thin pillars and alloy atoms due to availability of effective phonon scattering centers and increased probability of phonon annihilation in the pillar array structure film.

The layered and the ordinary Ag films are shown in Fig. 3. The cross-sectional SEM micrograph of the layered film confirms that the film possesses clearly layered microstructure, indicating that the grains obviously grow along the planar direction at 350 °C deposition temperature (Fig. 3a). As seen from this figure, the film is formed of a stack of a large number of layers in the planar direction, each with thickness of ~50 nm. The nano-layers are similar as a parallel micro channels for electrons in-plane transport. For the relatively high 350 °C deposition temperature, the nucleation in the vertical direction is slower than the in-plane crystal growth. The deposited atoms have more energy for lateral movement on the surface, leading to enhanced mobility of atoms to overcome surface diffusion barriers, which may be beneficial for migration of deposited atoms to in-plane growth. By controlling growth parameters, the microstructure of the film obviously changed, as shown in Fig. 3. For deposition temperature of 250 °C, the ordinary structure Ag film is obtained (Fig. 3b), which is composed of numerous bulk-like particles.

Subsequently, the in-plane transport properties of the $Bi_2Te_{2.7}Se_{0.3}$ pillar array were studied at room temperature, such as, the concentration and mobility of carriers, the electrical conductivity, the Seebeck coefficient, and the thermal conductivity, as shown in Table 1. The $Bi_2Te_{2.7}Se_{0.3}$ pillar array is expected to be characterized by high ZT~0.95 at room temperature because of its unique build-up structure. In addition, the in-plane electrical conductivities of the films investigated by a ZEM-3 show that the layered and the ordinary Ag films have the electrical conductivities of 8.6×10^7 S/m and 7.3×10^7 S/m at room temperature, respectively. These films may provide excellent properties for fabrication of a planar micro-device near room temperature.

Thus, the $Bi_2Te_{2.7}Se_{0.3}$ and Ag films were then introduced into a TE micro-device using mask-assisted deposition technology. Fig. 4a shows a photograph of 38 legs planar device constituted by *n*-$Bi_2Te_{2.7}Se_{0.3}$ pillar array elements in parallel. Fig. 4b shows an enlarged SEM image of the selected area marked by a square in

Table 1
Transport properties of $Bi_2Te_{2.7}Se_{0.3}$ pillar array measured at room temperature.

Pillar array	Carrier concentration ($10^{19}/cm^3$)	Carrier mobility ($cm^2/V{\cdot}s$)	Electrical conductivity (10^4 S/m)	Seebeck coefficient (μV/K)	Thermal conductivity (W/m·K)	ZT ~300 K
$Bi_2Te_{2.7}Se_{0.3}$	−5.7	71	6.5	−208	0.89	0.95

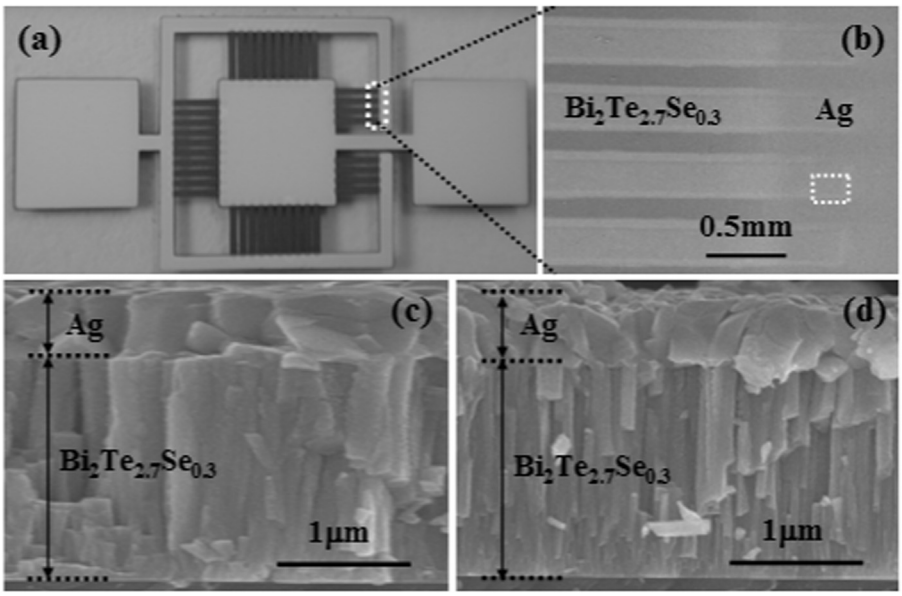

Fig. 4. (a) Photograph of planar $Bi_2Te_{2.7}Se_{0.3}$ pillar array device connected electrically in parallel; (b) SEM image of the selected area marked by the square in (a); (c) SEM image of the layered electrode related TE legs for the position marked by the square in (b) with cross-sectional view; (d) SEM image of the ordinary electrode related TE legs for the similar position as shown in (b) with cross-sectional view.

Fig. 4a. It further exhibits that this detailed morphology of the Ag electrode/TE pillar array interconnects applied to ensure good electrical contact, which is the key to guaranteeing good device performance. Besides, the surface of the legs in Fig. 3b shows that the $Bi_2Te_{2.7}Se_{0.3}$ pillar array and Ag films does not peel off the substrate, showing good adhesive strength between the films and the SiO_2 substrate based on van der Waals bonding.

Fig. 4c displays the cross-section SEM image of the bilayer structure for Ag/$Bi_2Te_{2.7}Se_{0.3}$ film leg ends, corresponding to the pillar array device with layered electrode. It is observed that $Bi_2Te_{2.7}Se_{0.3}$ pillar array and layered Ag films have been successfully incorporated into the micro-devices. The cross-sectional SEM micrograph of the TE legs confirms that the $Bi_2Te_{2.7}Se_{0.3}$ film possesses a clearly pillar array microstructure, obviously indicating that the grains preferentially grow along the (0 1 5) direction. It further exhibits detailed morphology of the layered Ag electrode/TE $Bi_2Te_{2.7}Se_{0.3}$ film interconnects applied to ensure electrical contact, which it would have an impact on device performance. For comparison, a pillar array device with ordinary electrode was also fabricated. A cross-sectional SEM of the leg ends is shown in Fig. 4d. The EDX results confirm that the atomic ratios are quite similar to those of the $Bi_2Te_{2.7}Se_{0.3}$ target in these TE films.

Next, the performance of pillar array devices was measured. The internal resistances (R_{in}) of the devices were obtained by a voltammetry method. The R_{in} value of the device with layered electrode is 2.4 Ω (Table 2), which is much smaller than that of the device with ordinary electrode (3.9 Ω). The resistance (R_f) of the film materials in the devices is calculated according to the similar method described by Francioso et al. [8]. The R_f value is about 2.1 Ω owing to high electrical conductivity of the pillar array material in both devices. The electrical contact resistance ($R_c = R_{in} - R_f$) of the interconnection between the electrode and TE film is about 0.3 Ω or 1.8 Ω for the device with layered or ordinary electrode, respectively. This implies that the layered structuring process possibly induces a favorable change in the Fermi surface topology of Ag electrode to significantly improve the electrical contact resistance.

To measure the open output voltage under a temperature difference for the device, one side of the TE element was heated and the other side was cooled using a self-made adapted characterization appliance as shown in previous work [15]. The temperature gradient was imposed parallel to the length of the TE legs. The output voltages of the device were obtained by a DC digital voltage meter. The maximum output power was estimated from the open output voltage and internal resistance of the device.

Fig. 5 shows the variation of the open output voltage (V_{op}) and output power (P_{max}) with temperature difference applied across the devices. As seen from Fig. 5, V_{op} approximately linearly

Table 2
The highest open output voltage, output power and cooling performance of pillar array device with layered or ordinary electrode.

Devices (electrode)	R_{in} (Ω)	R_c (Ω)	Power-generator			Cooler	
			ΔT (K)	V_{op} (mV)	P_{max} (μW)	I(mA)	ΔT_{max}(K)
Layered	2.4	0.3	65	12.4	16.02	50	11.1
Ordinary	3.9	1.8	65	7.2	3.32	60	6.8

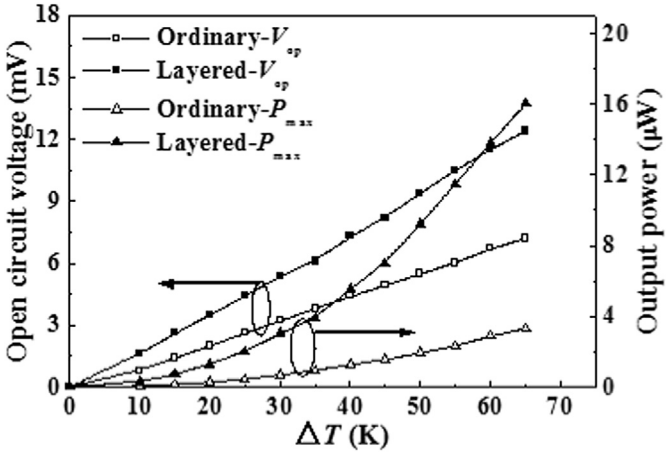

Fig. 5. Open output voltage and output power for pillar array device with layered or ordinary electrode as a function of applied temperature difference (ΔT).

increases with the temperature difference, which also implies that Seebeck coefficient (S) approximately remains constant with test temperature. Unlike for bulk Bi_2Te_3-based materials, whose Seebeck coefficients decrease as temperature increases. The temperature stability of S of the $Bi_2Te_{2.7}Se_{0.3}$ pillar array is useful when the TE device is in practical use. Compared with the pillar array device with ordinary electrode, the V_{op} and P_{max} values of the pillar array device with layered electrode are greatly enhanced.

The highest values of V_{op} and P_{max} obtained for the pillar array device with layered electrode used as a power generator are 12.4 mV and 16.02 μW at $\Delta T = 65$ K, respectively (Table 2). P_{max} of the device with layered electrode reaches about 5 times larger than that of the device with ordinary electrode at $\Delta T = 65$ K. This implies that the electrical contact resistance decreases due to the pillar array leg ends wrapped by layered Ag electrode film, thus greatly enhancing the performance of TE micro-device. For comparison, some devices integrating Bi–Sb–Te-based TE films are shown in Table 3. The presented pillar array device shows much better performance. However, these reported devices have some other advantages, for example, excellent V_{op} and good design concept, but with the drawback of low ZT values of TE materials and parasitic resistances. However, the presented device with layered electrode possesses relatively high ZT and low R_{in}, leading to improved P_{max}. This greatly enhanced thermoelectric device performance owing to synergistic effect between ordered $Bi_2Te_{2.7}Se_{0.3}$ pillar array and layered Ag electrode. However, the measured output voltages of the devices are lower than the predicted results based on the Seebeck coefficient value of −208 μV/K for the $Bi_2Te_{2.7}Se_{0.3}$ pillar array. This may result from a structural anisotropy of films, thermal contact effect, heat loss problem [19], or electric losses at the interconnects because of the contact resistances.

Based on the Peltier effect, the electrons in the Ag/$Bi_2Te_{2.7}Se_{0.3}$ junction will absorb sufficient energy to be transported to a higher energy level as the driving current flows from one side of the n-$Bi_2Te_{2.7}Se_{0.3}$ leg toward the other side. Therefore, this junction will serve as a heat absorber. At room temperature, cooling of the devices was examined without any forced heat removal by blowing air or running water at the heat sink, and all tests were repeated 10 times. Fig. 6 shows the variation of temperature difference between the hot and cold end resulting from the Peltier effect, as a function of input current for the devices. It is noticed that ΔT increases with increasing current to a certain optimum value of current, then slowly decreases. When a current was 50 mA, the 38 n-$Bi_2Te_{2.7}Se_{0.3}$ pillar array legs device with layered electrode has 5.6 K of cooling (down to 19.4 °C) and $\Delta T_{max} = 11.1$ K at an ambient temperature of about 25 °C. In theory, TE device cooling capacity is expressed as: [20]

$$Q_c = \alpha I T_c - \frac{1}{2} I^2 R_e - K(T_h - T_c) \quad (1)$$

where Q_c is the heat power absorbed at the device cold side; α is the Seebeck coefficient; I is the electric current of the device; R_e is the electric resistance of thermoelements; K is the thermal conductance of thermoelements; T_c, T_h are the temperatures of the cold and hot sides of the TE elements, respectively. When differential $dQ_c/dI = 0$, the value of the electric current yields:

$$I_{max} = \frac{\alpha T_c}{R_e} \approx 29.7\ mA \quad (2)$$

This calculated value of the electric current is lower than experimental result possibly due to the influence of SiO_2 substrate and thermal radiation of large surface areas of thermoelements. Compared with the device with ordinary electrode, good cooling by a TE device with layered electrode is associated with small R_{in} (Fig. 6; Table 2). This further confirms that the layered structure electrode can be beneficial for improving the performance of the planar device. In comparison with previous research [10–12,21], it is noted that the previously reported devices possess low TE film thermopower and high device electrical resistance, which degrade the cooling produced these devices. These adverse factors are improved in our device, enabling the device connected electrically in parallel to show relatively good cooling performance. It implies that a remarkably enhanced performance could be achieved in pillar array device with layered electrode through coordinate regulation between thermoelectric pillar array and layered electrode structures. In the case where the temperature of the cold junction is fixed and thermally insulated, according to $\Delta T_{max} = 0.5ZT_c^2$, the evaluated value may be higher than the measured result of 11.1 K. A factor that should be considered in micro-coolers is heat conduction along the metal wire to the cold side of the device [21]. This will reduce the maximum cooling. The thermal conductance of the substrate, the cooling power loss from the side contact, and radiation losses due to the large surface areas of the thermoelements deteriorate the operating performance. In

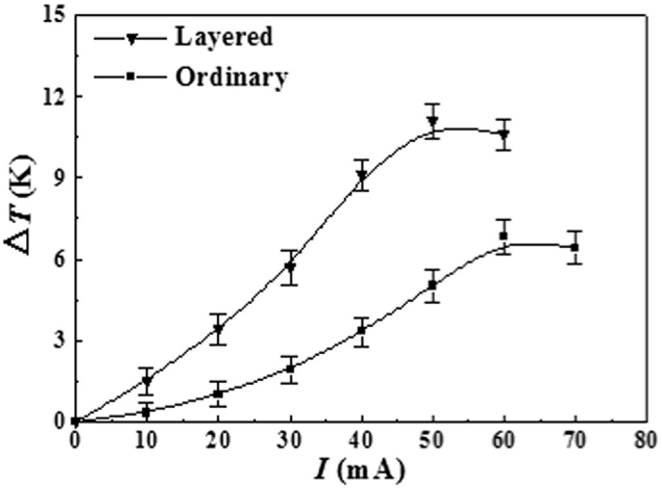

Fig. 6. Temperature difference (ΔT) versus input current for pillar array device with layered or ordinary electrode.

Table 3
The power generation performance of Bi–Sb–Te-based devices.

Devices	Leg-size			Power-generator			References
	Length (mm)	width (mm)	Thickness (μm)	ΔT (K)	V_{op} (mV)	P_{max} (μW)	
38-n	2.5	0.2	2	65	12.4	16.02	Our work
100-pair-of-n/p	2	0.25/0.425	0.5	40	430	0.032	[8]
242-pair-of-n/p	100 μm (diameter) × 20 μm (thickness)			22.3	294	5.9	[9]
7-pair-of-n/p	15	1	1	30	83.3	0.21	[16]
20-pair-of-n/p	12	0.2	4	45	/	1.3	[17]
11-pair-of-n/p	12 mm × 12 mm (device area)			50.6	/	1.9	[18]

addition, the results are lower than the predicted results due to the electrical contact resistances between the metallic junctions and TE elements. It is expected that these electrical contact resistances could be reduced by using a Ti/Au interface layer in the fabrication process [22]. The columnar structure electrode is similar as a parallel microchannel which can create some sort of channels for the easy transport of electrons and phonons in the device, possibly leading to further improve the electrical contact resistance [23]. The optimized aspect ratio of the thermoelements also remains to be explored. Additionally, the properties of materials should be further improved by controlling ordered lattice, pillar diameter, layer thickness, etc.

4. Conclusion

Highly ordered vertical *n*-$Bi_2Te_{2.7}Se_{0.3}$ pillar array and layered structure Ag films showed a promising in-plane property. 38 *n*-$Bi_2Te_{2.7}Se_{0.3}$ pillar array legs micro-device with layered Ag electrode was successfully fabricated using the magnetron sputtering and mask-assisted deposition technology. A remarkably enhanced performance could be achieved in pillar array device with layered electrode owing to synergistic effect between thermoelectric pillar array and layered electrode structures. For the pillar array device with layered electrode, the output voltage and maximum power were up to 12.4 mV and 16.02 μW, respectively, for a temperature difference of 65 K. The device could produce a 11.1 K maximum temperature difference at current of 50 mA. Introduction of such uniquely ordered pillar array and layered electrode structures into planar micro-devices is therefore a very promising approach.

Acknowledgments

This work was supported by the Science and Technology Development Fund Planning Project for the Universities of Tianjin (Grant no. 20130304), Scientific Research Fund Project of Tianjin University of Science and Technology (No. 20130121), State Key Development Program for Basic Research of China (No. 2012CB933200), National Natural Science Foundation of China (No. 61474082), Research Fund for Doctor Station Sponsored by the Ministry of Education of China (No. 20111102110035).

References

[1] Montecucco A, Knox AR. Accurate simulation of thermoelectric power generating systems. Appl Energy 2014;118:166–72.
[2] Bell LE. Cooling, heating, generating power, and recovering waste heat with thermoelectric systems. Science 2008;321:1457–61.
[3] Goncalves LM, Couto C, Alpuim P, Rolo AG, Völklein F, Correia JH. Optimization of thermoelectric properties on Bi_2Te_3 thin films deposited by thermal co-evaporation. Thin Solid Films 2010;518:2816–21.
[4] Majumdar A. Thermoelectric devices: helping chips to keep their cool. Natu Nanotech 2009;4:214–5.
[5] Fan P, Zheng ZH, Cai ZK, Chen TB, Liu PJ, Cai XM, et al. The high performance of a thin film thermoelectric generator with heat flow running parallel to film surface. Appl Phys Lett 2013;102:033904.
[6] Rowe DM. Thermoelectrics handbook: macro to nano. New York: Taylor & Francis Ltd; 2006.
[7] Ali H, Sahin AZ, Yilbas BS. Thermodynamic analysis of a thermoelectric power generator in relation to geometric configuration device pins. Energy Conv Mana 2014;78:634–40.
[8] Francioso L, Pascali CD, Farella I, Martucci C, Cretì P, Siciliano P, et al. Flexible thermoelectric generator for ambient assisted living wearable biometric sensors. J Power Sources 2011;196:3239–44.
[9] Kim MY, Oh TS. Thermoelectric power generation characteristics of a thin-film device consisting of electrodeposited *n*-Bi_2Te_3 and *p*-Sb_2Te_3 thin-film legs. J Electr Mater 2013;42:2752–7.
[10] Snyder GJ, Lim JR, Huang CK, Fleurial JP. Thermoelectric microdevice fabricated by a MEMS-like electrochemical process. Nat Mater 2003;2:528–31.
[11] Huang IY, Lin JC, She KD, Li MC. Development of low-cost micro-thermoelectric coolers utilizing MEMS technology. Sensors Actuat A-Phys 2008;148:176–85.
[12] Silva LWD, Kaviany M. Fabrication and measured performance of a first generation microthermoelectric cooler. J Microelectromech Syst 2005;14:1110–7.
[13] Tan M, Wang Y, Deng Y, Zhang ZW, Luo BW, Yang JY. Oriented growth of A_2Te_3 (A=Sb,Bi) films and their devices with enhanced thermoelectric performance. Sens Actuat A-Phys 2011;171:252–9.
[14] Kato R, Maesono A, Tye RP. Thermal conductivity measurement of submicron thick films deposited on substrates by modified ac calorimetry. Inter J Thermophys 2001;22:617–25.
[15] Tan M, Deng Y, Wang Y, Zhang ZW, Luo BW, Lin Z. Improved performance of thermoelectric micro-device by integrating a layered Bi_2Te_3 film. Thin Solid Films 2013;548:526–32.
[16] Takashiri M, Shirakawa T, Miyazaki K, Tsukamoto H. Fabrication and characterization of bismuthetelluride-based alloy thin film thermoelectric generators by flash evaporation method. Sensors Actuat A-Phys 2007;138:329–34.
[17] Kwon SD, Ju BK, Yoon SJ, Kim JS. Fabrication of bismuthetelluride-based alloy thin film thermoelectric deices grown by metal organic chemical vapor deposition. J Electr Mater 2009;38:920–5.
[18] Shin W, Nakashima T, Nishibori M, Izu N, Itoh T, Matsubara I. Planar-type thermoelectric micro devices using ceramic catalytic combustor. Curr Appl Phys 2011;11:S36–40.
[19] Hsu CT, Huang GY, Chu HS, Yu B, Yao DJ. Experiments and simulations on low temperature waste heat harvesting system by thermo-electric power generators. Appl Energy 2011;88:1291–5.
[20] Abramzon B. Numerical optimization of the thermoelectric cooling devices. J Electr Packag 2007;129:339–47.
[21] Zhang YL, Chen YF, Gong CM, Yang JK, Qian RM, Wang YJ. Optimization of superlattice thermoelectric materials and microcoolers. J Microelectromech Sys 2007;16:1113–9.
[22] Lin WP, Wesolowski DE, Lee CC. Barrier/bonding layers on bismuth telluride (Bi_2Te_3) for high temperature thermoelectric modules. J Mater Sci Mater Electron 2011;22:1313–20.
[23] Tan M, Deng Y, Hao YM. Improved thermoelectric performance of a film device induced by densely columnar Cu electrode. Energy 2014;70:143–8.